Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **BAL**
2. **– IN**
3. **+ IN**
4. **V -**
5. **BAL**
6. **OUT**
7. **V +**
8. **COMP**

**7**

**6**

**5**

**1 8**

**2**

**3**

**4**

**.050”**

**.065”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Unbiassed**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .050” X .065” DATE: 8/25/21**

**MFG: HARRIS THICKNESS .019” P/N: HA0-2515-6**

**DG 10.1.2**

#### Rev B, 7/1